What is claimed is:

1. A bus comprising:

a transmission line;

a pMOSFET driver to drive the transmission line, the pMOSFET driver having a source connected to a voltage source so as to be biased to a voltage V_{CC}; and

at least one termination device connecting the transmission line to ground.

2. The bus as set forth in claim 1, wherein the voltage V_{CC} is a core voltage.

3. The bus as set forth in claim 1, wherein each at least one termination device comprises a resistor connecting the transmission line to ground.

4. The bus as set forth in claim 1, wherein each at least one termination device comprises an nMOSFET coupling the transmission line to ground.

5. The bus as set forth in claim 1, wherein each at least one termination device is connected to the transmission line so as to provide a quiescent voltage of V_{SS} if the pMOSFET driver is OFF.

6. The bus as set forth in claim 5, wherein the voltage V_{CC} is a core voltage.

7. The bus as set forth in claim 1, the transmission line having two ends, wherein the at least one termination device comprises two resistors, each resistor connecting one end of the transmission line to ground, wherein the pMOSFET has a drain connected to the transmission line.

8. An electronic system comprising:

an integrated circuit having a substrate voltage V_{SS} and a voltage V_{CC};

a voltage source to provide the voltage V_{CC};

a transmission line having an end;

an agent connected to the transmission line;

a pMOSFET driver connected to the transmission line to communicate with the agent, the pMOSFET driver having a drain connected to the transmission line and having a source connected to the voltage source so as to be biased at the voltage V_{CC}; and

a termination device connected to the end of the transmission line to reduce signal reflection.

9. The electronic system as set forth in claim 8, wherein the voltage V_{CC} is a core voltage.

10. The electronic system as set forth in claim 8, wherein the termination device is connected to the transmission line so as to provide a quiescent voltage substantially equal to V_{SS} if the pMOSFET driver is OFF.

11. The electronic system as set forth in claim 10, wherein the voltage V_{CC} is a core voltage.

12. The electronic system as set forth in claim 8, wherein the termination device comprises at least one resistor connected to ground.

13. The electronic system as set forth in claim 8, wherein the termination device comprises at least one nMOSFET having a source connected to ground.

14. A bus comprising:

a transmission line;

a pMOSFET driver having a drain connected to the transmission line and a source at a voltage V_{CC}; and

at least one termination device connecting the transmission line to ground.

15. The bus as set forth in claim 14, wherein the voltage V_{CC} is a core voltage.

16. A method to provide electrical communication to a first agent and to a second agent via a transmission line, the first agent having a voltage V_{CC} and a substrate voltage V_{SS}, the method comprising:

exciting the transmission line in response to the first agent by switching ON a pMOSFET having a drain connected to the transmission line and a source at the voltage V_{CC};

reducing signal reflection from an end of the transmission line by providing at least one termination device connecting the transmission line to a source providing the substrate voltage V_{SS}; and

exciting the transmission line in response to the first agent by switching OFF the pMOSFET.

17. The method as set forth in claim 16, wherein the voltage V_{CC} is a core voltage.

18. A bus comprising:

a transmission line;

a pMOSFET driver to drive the transmission line, the pMOSFET driver having a source connected to a voltage source so as to be biased to a voltage V_{CC};

a nMOSFET driver coupled to the transmission line, the nMOSFET driver having a source at a substrate voltage V_{SS}; and

a combinational logic circuit coupled to the nMOSFET driver.

19. The bus as set forth in claim 18, wherein the combinational logic circuit is coupled to the nMOSFET driver so that the nMOSFET driver has a first ON resistance when the pMOSFET driver is ON and a second ON resistance when the pMOSFET driver is OFF, wherein the first and second ON resistances are not equal to each other.

20. The bus as set forth in claim 18, wherein the voltage V_{CC} is a core voltage.

21. The bus as set forth in claim 18, wherein the pMOSFET driver and nMOSFET in combination have an impedance substantially matched to the transmission line if both the pMOSFET driver and nMOSFET driver are switched ON, and wherein the nMOSFET has an impedance substantially matched to the transmission line if the pMOSFET driver is switched OFF.